

Amendments to the Specification:

On page 2, please replace:

“FIGURE 3 is an illustration of an example PLL arrangement for a converter;

FIGURES 4A - 4C are illustrations of various waveforms during the operation of a converter; and

FIGURE 5 illustrates an example embodiment of a boost converter, arranged in accordance with at least one aspect of the present invention.”

With the following:

“FIGURE 3 is an illustration of an example PLL arrangement for a converter;

FIGURES 4A - 4C are illustrations of various waveforms during the operation of a converter;

FIGURE 5 illustrates an example embodiment of a boost converter; and

FIGURES 6A – 6C illustrate various one-shot circuits, arranged in accordance with at least one aspect of the present invention.”

On page 4, please replace the paragraph from lines 24 – 30 as follows:

“The one-shot circuit can be any appropriate circuit (See e.g., FIGURES 6A – 6C) that is arranged to provide a pulse in response to a start signal. In one example, the one-shot circuit is simply an RS-type flip-flop circuit, where the start signal input corresponds to the set input (S). In another example, the one-shot circuit comprises an RS-type flip-flop circuit that is arranged to cooperate with a delay circuit. For this example, the flip-flop is set via the START signal, the delay circuit is initiated via the START signal, and the flip-flop is reset via an output of the delay circuit (See e.g., FIGURES 6B – 6C).”

On pages 6 - 7, please replace the paragraph from lines 23 – 30 and 1- 2 as follows:

“For a buck converter, the duty cycle of the converter circuit is given as: duty cycle = $V_{OUT}/V_{IN} = t_{ON}*f_{FB}$. As described previously, the one-shot circuit has a delay that can be implemented (or modeled) as a current (I_{OS}) that is fed into a capacitor (C_{OS}) to generate a voltage ramp (e.g., see FIGURE 6C). Current I_{OS} has a level that is set by I_{BIAS} . The rate of the voltage ramp ($\Delta V/\Delta t$) on the capacitor (C_{OS}) is determined by the level of current I_{OS} and the value of capacitor C_{OS} . Changes in the on-time interval (Δt_{ON}) for the converter corresponds are determined as: $\Delta t_{ON} = \Delta V_{OS} * C_{OS} / I_{BIAS} = \Delta V_{OS} * C_{OS} / I_{PLL}$, where: $I_{PLL} = V_{BIAS} * g_{mPLL}$, ΔV_{OS} corresponds to the change in voltage on capacitor C_{OS} , and g_{mPLL} corresponds to the transconductance associated with the buffer in the PLL circuit.”